In the claims:

1. (currently amended) A computer system for transferring ~~messages~~ data between a receiving central processing unit (CPU) and a transmitting CPU by using only write operations therebetween for the purpose of avoiding a direct read operation ~~between said receiving CPU and said~~ by the transmitting CPU from the receiving CPU, said system comprising:

a) at least one receiving central processing unit (CPU) comprising at least a read head register, a first queue length register, and a first total read register;

b) at least one transmitting CPU comprising at least a write head register, a second total read register, a total write register, and a second queue length register;

c) a local memory for said receiving CPU;

d) a local memory for said transmitting CPU;

e) means for connecting between said receiving CPU and said transmitting CPU where such means transfers write operations faster than read operations; ~~and~~

f) a circular queue defined between designated addresses in said local memory of said receiving CPU, wherein said read head register contains a pointer to the location of the next read from said circular queue and said write head register contains a pointer to the location of the next write into said circular queue;

g) means for periodically updating said second total read register with the content of said first total read register; and

h) means for adding and updating at least a message separator between messages, ~~wherein~~ such that said

transmitting CPU performs a read operation ~~of~~ from said receiving CPU ~~is achieved when said transmitting CPU performs~~ by the performance of:

1) a write operation providing a separator to said local memory of said receiving CPU at a location pointed to by said write head register~~; and~~, and

~~2) a write operation of~~ at least one message to said local memory of said receiving CPU at a location pointed to by said write head register, requesting data to be read by said transmitting CPU, and

~~3)~~ 2) a write operation performed by said receiving CPU to said transmitting CPU containing said data to be read by said transmitting CPU.

2. (deleted)

3. (deleted)

4. (currently amended) The system of claim 1 wherein said means for connecting between ~~said~~ said receiving CPU and said transmitting CPU is a PCI bus.

5. (deleted)

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9. (deleted)

10. (previously amended) The system of claim 1 wherein said read head register and said write head register are set to point to the same address upon initialization.

11. (previously amended) The system of claim 1 wherein a maximum length is imposed on a message to be written into said circular queue.

12. (previously amended) The system of claim 11 wherein a tail is added at the end of said circular queue, said tail being equal in length to said maximum length imposed on said message.

13. (previously amended) The system of claim 1 wherein a header separator is used to indicate the end of said message.

14. (previously amended) The system of claim 13 wherein said header separator contains the length of the immediately following message.

15. (previously amended) The system of claim 13 wherein said header separator contains a predefined header "magic" number.

16. (previously amended) The system of claim 15 wherein, if said header separator contains an erroneous header "magic" number, an error message is generated.

17. (previously amended) The system of claim 13 wherein a separator of the last message in said queue is a stopper separator, and is different from said header separator placed between subsequent messages.

18. (previously amended) The system of claim 17 wherein said stopper separator further contains a predefined stopper "magic" number.

19. (previously amended) The system of claim 18 wherein, if a stopper separator contains an erroneous stopper "magic" number, an error message is generated.

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